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AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Canceled)

2. (Previously Presented) The integrated circuit device of claim 16, wherein a plane of the carrier device die paddle is in said device plane, and wherein the stamped pedestals have pedestal sidewalls with an angle (α) greater than 45 degrees with respect to said device plane.

3. (Previously Presented) The integrated circuit device of claim 16, wherein the top surface of the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device and each top surface has an area for connection of a single bonding wire.

4. (Previously Presented) The integrated circuit device of claim 16, wherein said pedestal height of each of the stamped pedestals lies in the range between 1/10 and 1.5 times of a height of the semiconductor die.

5. (Previously Presented) The integrated circuit device of claim 16, wherein said pedestal height of each of the stamped pedestals lies in the range between 1/5 to twice a material thickness (h) of the carrier device.

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6. (Previously Presented) The integrated circuit device of claim 16, wherein each of the stamped pedestals is a local deformation of the metal layer of the carrier device which is formed by a punch device.

7. (Previously Presented) The integrated circuit device of claim 16, wherein at least one additional pedestal is formed by application of material to the carrier device.

8. (Previously Presented) The integrated circuit device of claim 16, wherein a silver or gold finish is on the stamped pedestals.

9. – 12. (Canceled)

13. (Previously Presented) The integrated circuit device of claim 17, wherein the sidewalls of the stamped pedestals make an angle (α) greater than 45 degrees with the device plane of the carrier device, with the sidewalls having at their base rounded junctions with the device plane.

14. (Previously Presented) The integrated circuit device of claim 17, wherein the height of the stamped pedestals lies in the range between 1/10 to one times the die height.

15. (Previously Presented) The integrated circuit device of claim 16, wherein only in the areas of stamped pedestals, a finish, having at least one of silver or gold, is provided for bondability.

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16. (Currently Amended) An integrated circuit device, comprising:

a semiconductor die;

a carrier device comprising a die paddle having a support surface onto which the semiconductor die is attached, and a plurality of stamped pedestals arranged on a metal layer extending in a device plane exteriorly surrounding and adjacent to the die paddle, wherein the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;

a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion;

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion; and

a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portion,

wherein at least one of said stamped pedestals includes a sidewall having a face extending, upward from the device plane, from a pedestal base junction extending along a closed path on the device plane, to a pedestal top surface spaced a pedestal height above the device plane, the sidewall being continuous, at all points of the pedestal base junction, from the pedestal base junction to the pedestal top surface,

wherein the entirety of a base of each one of said pedestals is contiguous with the device plane, and

wherein a stamped depth of each of said pedestals does not exceed a plane

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formed along an upper surface of the pedestal base.

17. (Currently Amended) An integrated circuit device, comprising:

a semiconductor die;

a metallic carrier device comprising a planar surface onto which the semiconductor die is attached, and a plurality of stamped pedestals arranged on a metal layer extending in a device plane exteriorly surrounding and adjacent to the planar surface, wherein the carrier device and the stamped pedestals form a single piece unitary structure;

a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion; and

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion,

wherein at least one of said stamped pedestals includes a sidewall having a face extending, upward from the device plane, from a pedestal base junction extending along a closed path on the device plane, to a pedestal top surface spaced a pedestal height above the device plane, the sidewall being continuous, at all points of the pedestal base junction, from the pedestal base junction to the pedestal top surface, wherein the entirety of a base of the pedestal is contiguous with the device plane, and

wherein a stamped depth of each of said pedestals does not exceed a plane formed along an upper surface of the pedestal base.

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18. – 23. (Canceled)

24. (Previously Presented) The integrated circuit device of claim 16, wherein the metallic leads are separate from the carrier device.

25. (Previously Presented) The integrated circuit device of claim 17, wherein the metallic leads are separate from the metallic carrier device.

26. (Previously Presented) The integrated circuit device of claim 16, wherein said semiconductor die has a side surface extending from a bottom surface to a top surface, said side surface extending along a rectangular perimeter lying in the device plane, said rectangular perimeter having a first side, a second side parallel to and spaced from said first side, and a third side normal to said first side, wherein a first of said stamped pedestals is located adjacent said first side, a second of said stamped pedestals is located adjacent said second side, and a third of said stamped pedestals is located adjacent said third side.

27. (Previously Presented) The integrated circuit device of claim 26, wherein said semiconductor die has a further side surface parallel to and spaced from said third side surface, and wherein at least one of said stamped pedestals is located adjacent said fourth side.

28. (Previously Presented) The integrated circuit device of claim 16, wherein said

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semiconductor die has a side surface extending from a bottom surface to a top surface, said side surface extending along a rectangular perimeter lying in said device plane, said rectangular perimeter having a first side, a second side parallel to and spaced from said first side, and a third side normal to said first side, wherein each of said plurality of said stamped pedestals is located adjacent said first side.

29. (Previously Presented) The integrated circuit device of claim 17, wherein said semiconductor die has a side surface extending from the bottom surface to the top surface, said side surface extending along a rectangular perimeter lying in said device plane, said rectangular perimeter having a first side, a second side parallel to and spaced from said first side, and a third side normal to said first side, wherein a first of said stamped pedestals is located adjacent said first side, a second of said stamped pedestals is located adjacent said second side; and a third of said stamped pedestals is located adjacent said third side.

30. (Previously Presented) The integrated circuit device of claim 29, wherein said semiconductor die has a further side surface parallel to and spaced from said third side surface, and wherein at least one of said stamped pedestals is located adjacent said fourth side.

31. (Previously Presented) The integrated circuit device of claim 17, wherein said semiconductor die has a side surface extending from the bottom surface to the top surface, said side surface extending along a rectangular perimeter lying in said device

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plane, said rectangular perimeter having a first side, a second side parallel to and spaced from said first side, and a third side normal to said first side, wherein each of said plurality of said stamped pedestals is located adjacent said first side.

32. (Currently Amended) An integrated circuit device, comprising:

a carrier having a die support surface extending in a support plane, and a plurality of stamped pedestals surrounding and adjacent to the die support surface, each pedestal projecting a pedestal height above the support plane;

a semiconductor die attached to the die support surface of the carrier, having a top surface located a die height above the support plane, and a plurality of bond pads on an area of the top surface;

a lead finger supported to have one end proximal at least one of said stamped pedestals, extending away from the semiconductor die;

a first bond wire extending from one of said bond pads to one of said at least one stamped pedestals proximal the one end of the lead finger; and

a second bond wire extending from said one of said stamped pedestals to said one end of said lead finger,

wherein said pedestal height is in the range between 1/5 and 1/ 2 of said die height, and

wherein a stamped depth of each of said pedestals does not exceed a plane formed along an upper surface of the pedestal base.

33. (Previously Presented) The integrated circuit device of claim 32, wherein at least

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one of the pedestals has a pedestal top planar surface located at the pedestal height of said at least one pedestal above the support plane.

34. (Previously Presented) The integrated circuit device of claim 33, wherein said first bond wire and said second bond wire each attach to said pedestal top planar surface.

35. (Previously Presented) The integrated circuit device of claim 32, wherein the die support surface is a surface of a portion of a carrier platform structure, and at least one of the pedestals comprises a pedestal structure attached to the carrier platform structure.

36. (Previously Presented) The integrated circuit device of claim 32, wherein all of the pedestals have the same pedestal height.

37. (Cancelled)

38. (Previously Presented) The integrated circuit device of claim 37, having a non-bonded pedestal, said non-bonded pedestal having no bond wire attached, and having one continuous laminated structure with a first portion forming said die support and a second portion forming said non-bonded pedestal.

39. (Previously Presented) The integrated circuit of claim 33, wherein portions of said carrier have a first finish and said planar top surfaces have a second finish different

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from said first finish.

40. (Previously Presented) The integrated circuit device of claim 39, wherein said second finish includes a metal from the group consisting of gold and silver.

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